CLAIMS

1. A method for manufacturing an integrated circuit, the method comprising:

(1) obtaining a structure comprising:

a semiconductor substrate having one or more first areas which are to include one or more active areas of one or more nonvolatile memory cells;

one or more dielectric regions abutting the one or more first areas and rising above the substrate, each of said dielectric regions having a sidewall abutting at least one of the first areas, wherein at least a top portion of the sidewall is exposed;

(2) etching at least the top exposed portion of each sidewall of each said dielectric region, to recess the top portion of the sidewall laterally away from the adjacent first area;

(3) forming a first conductive layer over the one or more first areas, the first conductive layer being insulated from the one or more first areas, the first conductive layer abutting the top recessed sidewall portion of each said dielectric region and providing at least a portion of a floating gate for each nonvolatile memory cell.

2. The method of Claim 1 further comprising:

forming a dielectric layer on the first conductive layer;

forming a second conductive layer on the dielectric layer, to provide a control gate for each nonvolatile memory cell.

3. The method of Claim 1 wherein the operation (1) comprises:

forming one or more first structures on the one or more first areas, the one or more first structures covering said top portion of each said sidewall; and

etching the one or more first structures to expose said top portion of each said sidewall.

4. The method of Claim 1 wherein the operation (1) comprises:

forming a layer L1 on the semiconductor substrate;

patterning the layer L1 to form one or more first structures on the one or more first areas and expose the substrate in areas in which the dielectric regions are to be formed;

forming the dielectric regions, wherein each said sidewall of each said dielectric region abuts, and is covered by, one of said first structures;

etching the one or more first structures to expose said top portion of each said sidewall.

5. The method of Claim 4 further comprising, after patterning the layer L1, etching one or more trenches in the substrate and filling the trenches with dielectric to form the one or more dielectric regions.

6. An integrated circuit comprising a semiconductor substrate and a nonvolatile memory cell having an active area formed in the semiconductor substrate, the memory cell comprising:

a dielectric on the active area; and

a floating gate on the dielectric, the floating gate having a horizontal top surface projecting laterally beyond the active area.

7. The integrated circuit of Claim 6 wherein at a location at which the top surface of the floating gate projects beyond the active area, the floating gate has a sidewall, and at least a top portion of the sidewall extends laterally outward and beyond the active area as the sidewall is traced upward.

8. The integrated circuit of Claim 7 further comprising a dielectric region abutting said top portion of the sidewall.

9. An integrated circuit comprising a semiconductor substrate and a nonvolatile memory cell having an active area formed in the semiconductor substrate, the memory cell comprising:

a dielectric on the active area; and

a floating gate on the dielectric, wherein the floating gate has a sidewall, and at least a top portion of the sidewall extends laterally outward as the sidewall is traced upward.

10. The integrated circuit of Claim 9 further comprising a dielectric region physically contacting, and extending along, said top portion of the sidewall.